IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: NEMAZIE et al.	Art Unit: 2181
Appl. No.: 10/775,521	Examiner: Lee, Chun Kaun
Filed: 02/09/2004	Atty. Docket: Siliconstor-002US
For: Switching Serial Advanced Technology Attachment (SATA) to a Parallel Interface	

Appeal Brief Under 37 CFR § 41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Final Office Action mailed December 11, 2007, Appellants submit this appeal brief under 37 CFR § 41.37.

The requisite fee of $510 under 37 CFR § 40 (B)(2) and any fees required under 37 CFR. 1. 136(a) for any extension of time required to submit this appeal brief, is sought to be submitted accompanying the filing of this appeal brief. However, the USPTO is directed to charge all required fees (except for the issue fees and the publication fees) to process the pending appeal and credit any overpayments to Deposit Account No. 12-2252.

Table of Contents

I. REAL PARTY IN INTEREST

This application is assigned to LSI Logic Corporation, by Virtue of the assignment recorded on 10/05/2007, at reel/frame 019927/0098.

II. RELATED APPEALS AND INTERFERENCES

This application claims priority to U.S. Patent Application No. 10/775,523, filed on February 9, 2004 and entitled "Route Aware Serial Advanced Technology Attachment (SATA) Switch", which is being appealed. An appeal brief in the foregoing case was filed on January 11, 2008. To the Applicants' knowledge, no decision has been rendered, to date.

III. STATUS OF CLAIMS

A. Pending Claims

Claims 1, 4-19, 22-32 and 35-43 are pending. Of these, claims 1, 18, and 31 are independent claims.

B. Rejections

All claims 11, 4-19, 22-32 and 35-43 were rejected.

In particular, claims 1, 4, 6-14, 18-19, 22-32 and 35-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" and Utsunomiya et al. (US Pub.:2003/0131166).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" and Utsunomiya et al. (US Pub.:2003/0131166) as applied to claims 1, 4, 6-14 and 18-43 above, and further in view of Boucher et al. (US Patent 6,434,620).

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA," Utsunomiya et al. (US Pub.:2003/0131166) and "Serial ATA Specification."

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA," Utsunomiya et al. (US Pub.:2003/0131166), and Shin et al. (US Patent 7,154,905).

Appealed Claims

All the pending claims 1, 4-19, 22-32 and 35-43 are subject of this appeal.

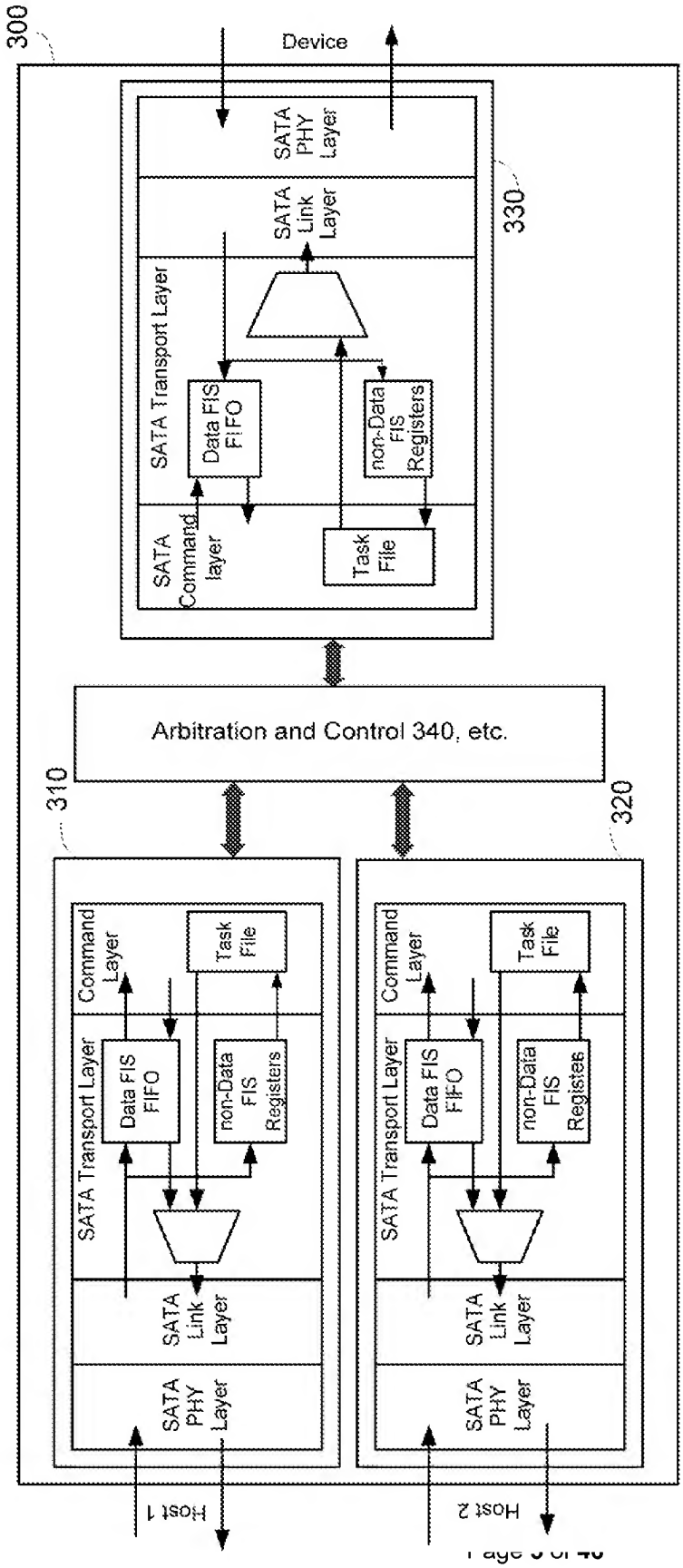
IV. STATUS OF AMENDMENTS

An amendment was filed on January 28, 2008, subsequent to the outstanding final rejection. This amendment was entered, as noted in the Advisory Action, issued on Feburary 8, 2008.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed subject matter relates to enabling multiple hosts to concurrently access a single storage device using industry-standard Serial Advanced Technology Attachment (SATA) interface protocol.

By way of convenience, an exemplary embodiment of the present invention is illustrated in the figure below, which is a condensed representation of Fig. 6 from the patent application.


300
Device
SATA PHY Layer
SATA Link Layer
330
SATA Transport Layer
Data FIS FIFO
non-Data FIS Registers
SATA Command layer
Task File
Arbitration and Control 340, etc.
310
320
Command Layer
Task File
SATA Transport Layer
Data FIS FIFO
non-Data FIS Registers
SATA Link Layer
SATA PHY Layer
Host 1
Host 2

In general, the switch 300 includes SATA ports 310 and 320, which are coupled to hosts 1 and 2, respectively. The switch 300 further includes SATA port 330, which is coupled to a Device. The Device is generally a storage device. The features of the various embodiments of the present invention allow the hosts concurrent access to the Device. Concurrency, as used herein, indicates acceptance of commands, from either of two or more hosts, at any given time including when the Device (such as a storage unit) is not in an idle state.

Turning now to the claimed subject matter, claim 1 is directed towards "a switch coupled between a plurality of host units and a device for communicating therebetween." Claim 1 recites in part "comprising: a first serial advanced technology attachment (ATA) port coupled to a first host unit and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit." Claim 1 further recites "a second serial ATA port coupled to a second host unit and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit." Claim 1 further recites "a third parallel ATA port, coupled to a device, for causing access to the device, by the first or second host units." Lastly, claim 1 includes "an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state."

Thus, various embodiments of the present invention innovatively teach using a host task file in each SATA port. It is noted that the first and second task files are located before the arbitration and control circuit therefore allowing concurrent acceptance of commands from the hosts.

Figure 12 of the instant specification show how, by using reserved bits in the FIS, the FIS organization can be modified to identify the host originating the FIS, making routing of the FIS transparent to the switch.

Claim 4 further defines the switch in claim 1 "wherein said third parallel ATA port includes a device task file.

Claim 5 further defines the switch in claim 4 "wherein said first, second and third ports are level 4 ports."

Claim 6 further defines the switch as recited in claim 1. Thus, claim 6 recites "wherein said device is a storage unit."

Claim 7 still further defines where the switch in claim 1 is employed. Thus, Claim 7 recites "wherein said switch is employed in an enterprise system."

Claim 8 further defines the switch as recited in claim 1 "wherein said arbitration and control circuit causes concurrent access to the device by the first and second host units."

Claim 9 further defines the switch in claim 1 "wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units."

Claim 10 further defines the switch in claim 9. Thus, claim 10 recites "wherein the information is referred to as 'identity drive response.'"

Claim 11 further defines the switch in claim 9 wherein "the information is referred to as 'Tag.'"

Claim 12 further defines the switch in claim 1 "wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device."

Claim 13 further defines the switch as recited in claim 12. Thus, claim 13 recites "wherein the information is referred to as 'Tag.'"

Claim 14 further defines the switch in claim 13 "wherein the arbitration and control circuit include a Tag/Sactive Mapping Circuit for mapping a host tag to a device tag and inverse mapping for identifying a host."

Claim 15 further defines the switch in claim 1 "wherein either the first or the second host sends a legacy queue command queued by the device."

Claim 16 further defines the switch in claim 1 "wherein either the first or the second host sends a native queue command for execution thereof by the device."

Claim 17 further defines the switch in claim 1 "wherein the first, second and third ports are level 3 ports and a Data frame information system (FIS) first-in-first-out (FIFO) and an associated FIFO Control are coupled to the first, second and third ports and located external thereto."

Claim 18 is directed towards a switch "comprising: a first serial advanced technology attachment (ATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit." Claim 18 further recites that the switch also includes "a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit." Claim 18 still further recites "a third parallel ATA port for connection to a device." Lastly, claim 18 states that the switch includes "an arbitration and control circuit, coupled to the first, second and third ports, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state."

Claim 19 further defines the switch in claim 18 wherein "the switch is a serial ATA switch."

Claim 22 further defines the switch in claim 18 "wherein said third parallel ATA port includes a device task file."

Claim 23 further defines the switch in claim 18 "wherein said device is a storage unit."

Claim 24 further defines the switch recited in claim 18 "wherein said switch is employed in an enterprise system."

Claim 25 further defines the switch in claim 18 "wherein said arbitration circuit causes concurrent access of the device by the first and second host units."

Claim 26 further defines the switch in claim 18 "wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units."

Claim 27 further defines the switch in claim 26 "wherein the information is referred to as 'identity drive response.'"

Claim 28 further defines the switch in claim 26 "wherein the information is referred to as 'Tag.'"

Claim 29 further defines the switch in claim 18. Thus, claim 29 recites "wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device."

Claim 30 further defines the switch in claim 28 "wherein the information is referred to as 'Tag.'"

Claim 31 is directed towards a switch "that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (SATA) links." Claim 31 further recites that the switch is comprised of "a first serial ATA port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host units." The switch in claim 31 is further comprised of "a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit." Claim 31 further recites the switch to include "a third

parallel ATA port for connection to a device." Lastly, claim 31 recites that the switch is also comprised of "an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state."

Claim 32 further defines the switch in claim 31 "wherein the switch is a serial ATA switch."

Claim 35 further defines the switch in claim 31 "wherein said third parallel ATA port includes a device task file."

Claim 36 further defines the switch in claim 31 "wherein said device is a storage unit"

Claim 37 further defines the switch in claim 31 "wherein said switch is employed in an enterprise system."

Claim 38 further defines the switch in claim 31 "wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units."

Claim 39 further defines the switch in claim 31 "wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units."

Claim 40 further defines the switch in claim 39. Thus, claim 40 recites "wherein the information is referred to as 'identity drive response.'"

Claim 41 further defines the switch in claim 39 "wherein the information is referred to as 'Tag.'"

Claim 42 further defines the switch in claim 31 "wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the

switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device."

Claim 43 further defines the switch in claim 42 "wherein the information is referred to as 'Tag.'"

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether the rejection of claims 1, 4, 6-14, 18-19, 22-32 and 35-43 under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" and Utsunomiya et al. (US Pub.:2003/0131166) is proper.

Whether the rejection of claim 5 under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" and Utsunomiya et al. (US Pub.:2003/0131166) as applied to claims 1, 4, 6-14 and 18-43 above, and further in view of Boucher et al. (US Patent 6,434,620) is proper.

Whether the rejection of claims 15-16 under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA," Utsunomiya et al. (US Pub.:2003/0131166) and "Serial ATA Specification" is proper.

Whether the rejection of claim 17 under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA," Utsunomiya et al. (US Pub.:2003/0131166), and Shin et al. (US Patent 7,154,905) is proper.

VII. Mapping of Specification to Drawings

The independent claims are listed below, and mapped to specifications by page and line number and to the drawings.

Claim 1

Claim 1: A switch coupled between a plurality of host units and a device for communicating therebetween and comprising:

a) a first serial advanced technology attachment (ATA) port coupled to a first host unit and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;

b) a second serial ATA port coupled to a second host unit and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;

c) a third parallel ATA port, coupled to a device, for causing access to the device, by the first or second host units; and

d) an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Subject Matter	Reference to Figs	Reference to Specs
A switch	Fig. 5 Block 200 Fig. 6 Block 300 Fig. 10a Bock 500 Fig. 10b Block 500	Page 13, line 7-line 12 Page 15, lines 28-32 Page 35, lines 19-25
coupled between a plurality of host units	Fig. 5 Block 210 Fig. 5 Block 220	Page 13, line 9 Page 13, lines 16-20 Page 13, lines 26-28

and a device for communicating therebetween and comprising:	Fig. 3a item 16 Fig. 3b item 66	Page 1, lines 20 - 21
a) a first serial advanced technology attachment (ATA) port coupled to a first host unit;	Fig. 5 Block 210 Fig. 6 Blocks 310 Fig. 9 Block 410 Fig. 10a Block 510 Fig. 10b Block 510	Page 13, line 16-Page 14, line 14 Page 15, line 29-Page 16, line 3 Page 27, lines 1-5 Page 34, line 18-Page 35, line 19
and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;	Fig. 6, block labeled "Task File" inside block 310 Fig. 9, block 413a Fig. 10a, block 513a Fig. 10b, block labeled "FIS Holding Reg" inside block 510	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11-13
b) a second serial ATA port coupled to a second host unit	Fig. 5 Block 220 Fig. 6 Block 320 Fig. 9 Block 410 Fig. 10a Block 520 Fig. 10b Block 520 Fig. 11a Block 320 Fig. 11b Block 520	Page 13, line 26-Page 14, line 3 Page 15, line 30-Page 16, line 7 Page 27, lines 6-10 Page 34, line 18-Page 35, line 19

and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;	Fig. 6 Block labeled "Task File" inside Block 310	Page 17, lines 19-20 Page 45, lines 5-6 Page 45, lines 11-13
c) a third parallel ATA port, coupled to a device, for causing access to the device, by the first or second host units; and	Fig. 5 Block 230 Fig. 6 Block 330 Fig. 10a Block 530 Fig. 10b Block 530	Page 14, lines 4-14 Page 16, lines 7-11 Page 37, lines 17-18
an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.	Fig. 10a(ii) Fig. 10b(ii) Fig. 11a(ii) Fig. 11b(i)	Page 16, lines 17-20 Page 16, line 25-Page 17, line 4 Page 17, line 18-Page 18, line 2 Page 18, lines 17-20 Page 24, lines 1-5 Page 24, lines 7-12 Page 26, lines 22-23 Page 37, line 25-Page 38, line 9 Page 38, lines 18-20 Page 38, lines 21-25 Page 38, lines 27-31 Page 39, lines 2-7

Claim 18

Claim 18: A switch comprising:

a. a first serial advanced technology attachment (ATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

b. a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

c. a third parallel ATA port for connection to a device; and

an arbitration and control circuit, coupled to the first, second and third ports, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Subject Matter	Reference to Figs	Reference to Specs
A switch comprising:	Fig. 5 Block 200 Fig. 6 Block 300 Fig. 10a Bock 500 Fig. 10b Block 500	Page 13, line 7-line 12 Page 15, lines 28-32 Page 35, lines 19-25
a first serial advanced technology attachment (ATA) port for connection to a first host unit,	Fig. 5 Block 210 Fig. 6 Blocks 310 Fig. 9 Block 410 Fig. 10a Block 510 Fig. 10b Block 510	Page 13, line 16-Page 14, line 14 Page 15, line 29-Page 16, line 3 Page 27, lines 1-5 Page 34, line 18-Page 35, line 19

the first port including a first host task file responsive to commands sent by the first host unit;	Fig. 6, block labeled "Task File" inside block 310 Fig. 9, block 413a Fig. 10a, block 513a Fig. 10b, block labeled "FIS Holding Reg" inside block 510	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11-13
b) a second serial ATA port for connection to a second host unit,	Fig. 5 Block 220 Fig. 6 Block 320 Fig. 9 Block 410 Fig. 10a Block 520 Fig. 10b Block 520 Fig. 11a Block 320 Fig. 11b Block 520	Page 13, line 26-Page 14, line 3 Page 15, line 30-Page 16, line 7 Page 27, lines 6-10 Page 34, line 18-Page 35, line 19
the second port including a second host task file responsive to commands sent by the second host unit;	Fig. 6, block labeled "Task File" inside block 320 Fig. 9, block 413a Fig. 10a, block 523a Fig. 10b, block labeled "FIS Holding Reg" inside block 520	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11-13
c) a third parallel ATA port for connection to a device;	Fig. 5 Block 230 Fig. 6 Block 330	Page 14, lines 4-14 Page 16, lines 7-11

	Fig. 10a Block 530 Fig. 10b Block 530	Page 37, lines 17-18
and an arbitration and control circuit, coupled to the first, second and third ports, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.	Fig. 10a(ii) Fig. 10b(ii) Fig. 11a(ii) Fig. 11b(i)	Page 16, lines 17-20 Page 16, line 25-Page 17, line 4 Page 17, line 18-Page 18, line 2 Page 18, lines 17-20 Page 24, lines 1-5 Page 24, lines 7-12 Page 26, lines 22-23 Page 37, line 25-Page 38, line 9 Page 38, lines 18-20 Page 38, lines 21-25 Page 38, lines 27-31 Page 39, lines 2-7

Claim 31

Claim 31: A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, said switch comprising:

a. a first serial ATA port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;
b. a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;
c. a third parallel ATA port for connection to a device; and

d. an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Subject Matter	Reference to Figs	Reference to Specs
A switch	Fig. 5 Block 200 Fig. 6 Block 300 Fig. 10a Bock 500 Fig. 10b Block 500	Page 13, line 7-line 12 Page 15, lines 28-32 Page 35, lines 19-25
that is connectable to a first host unit,	Fig. 3a item 11 Fig. 3b item 11	
a second host unit	Fig. 3a item 12 Fig. 3b item 12	
and a device	Fig. 3a item 16	Page 1, lines 20 - 21
via serial advanced technology attachment	Fig. 5, items 211rx	Page 13, lines 17 – 18,

(ATA) links, said switch comprising:	211tx, 231rx, 231tx, 221rd, 221tx Fig. 6, items 311rx, 311tx, 321rx, 321tx, 331rx, 331tx Fig. 9 items 411rx, 411tx Fig. 10a items 511tx, 511rx, 521tx, 521rx, 531tx, 531rx Fig. 10b items 511tx, 511rx, 521tx, 521rx, 531tx, 531rx	26 - 29 Page 14, lines 5- 7 Page 15, line 32 – page 16 line 9 Page 36, lines 1-2, 9-10, 17 – 18 Page 37, lines 1 - 2, 9-10, 17 - 18
a. a first serial ATA port	Fig. 5 Block 210 Fig. 6 Blocks 310 Fig. 9 Block 410 Fig. 10a Block 510 Fig. 10b Block 510	Page 13, line 16-Page 14, line 14 Page 15, line 29-Page 16, line 3 Page 27, lines 1-5 Page 34, line 18-Page 35, line 19
for connection of a first host unit,	Fig. 3a item 11 Fig. 3b item 11	
the first port including a first host task file responsive to commands sent by the first host unit;	Fig. 6, block labeled "Task File" inside block 310 Fig. 9, block 413a Fig. 10a, block 513a Fig. 10b, block	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11-13

	labeled "FIS Holding Reg" inside block 510	
b. a second serial ATA port	Fig. 5 Block 220 Fig. 6 Block 320 Fig. 9 Block 410 Fig. 10a Block 520 Fig. 10b Block 520 Fig. 11a Block 320 Fig. 11b Block 520	Page 13, line 26-Page 14, line 3 Page 15, line 30-Page 16, line 7 Page 27, lines 6-10 Page 34, line 18-Page 35, line 19
for connection to a second host unit,	Fig. 3a item 12 Fig. 3b item 12	
the second port including a second host task file responsive to commands sent by the second host unit;	Fig. 6 Block labeled "Task File" inside Block 310	Page 17, lines 19-20 Page 45, lines 5-6 Page 45, lines 11-13
c. a third parallel ATA port for connection to a device; and	Fig. 5 Block 230 Fig. 6 Block 330 Fig. 10a Block 530 Fig. 10b Block 530	Page 14, lines 4-14 Page 16, lines 7-11 Page 37, lines 17-18
d. an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.	Fig. 10a(ii) Fig. 10b(ii) Fig. 11a(ii) Fig. 11b(i)	Page 16, lines 17-20 Page 16, line 25-Page 17, line 4 Page 17, line 18-Page 18, line 2 Page 18, lines 17-20

		Page 24, lines 1-5 Page 24, lines 7-12 Page 26, lines 22-23 Page 37, line 25-Page 38, line 9 Page 38, lines 18-20 Page 38, lines 21-25 Page 38, lines 27-31 Page 39, lines 2-7

VIII. THE ARGUMENT

A. Brief Introduction to references cited by the examiner

As noted above, claims 1, 4, 6-14, 18-19, 22-32 and 35-43 were rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" and Utsunomiya et al. (US Pub.:2003/0131166).

Claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA" and Utsunomiya et al. (US Pub.:2003/0131166) as applied to claims 1, 4, 6-14 and 18-43 above, and further in view of Boucher et al. (US Patent 6,434,620).

Claims 15-16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA," Utsunomiya et al. (US Pub.:2003/0131166) and "Serial ATA Specification."

Claim 17 was rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) in view of "SATA vs. PATA: the reality of Serial and Parallel ATA-Serial ATA," Utsunomiya et al. (US Pub.:2003/0131166), and Shin et al. (US Patent 7,154,905).

A brief introduction to Grieff, Utsunomiya, "Serial ATA Specification," Shin, and Boucher is provided below.

1. Brief Introduction to *Grieff*

Grieff relates generally to a dual port adapter (DPA) for providing multi-initiator capability to a SATA drive. Grieff uses link-layer (or layer 2) ports on the host and device sides. For example, in Grieff, the host ports 130 and 132 are described to be Link Layer (layer 2) state machines. [Grieff: Col. 5, lines 50-56] Additionally, in Grieff, the arbiter module 112 is described to process at the Link Layer (layer 2). [See: Grieff, Col. 5, Lns. 50-56].

The host-side ports are specifically described to be state machines. [Grieff: Col. 5, lines 50-56.] In Grieff, an arbiter module connected directly to the host ports arbitrates between the two hosts on a round-robin scheme. [Id.] The host that wins arbitration is granted access. Thus, under Grieff, only one host is granted access to the device at any given time.

Once a host wins arbitration, commands issued by that host are routed through a mux and to an inbound decoder. [Grieff Col. 5, lines 25-30]. In the architecture proposed by Grieff, a host is not granted access, and cannot issue commands, until it has won arbitration.

In short, Grieff describes a DPA that uses layer-2 state machine ports to connect to multiple hosts. The DPA arbitrates between the two hosts, meaning only one host can communicate with the DPA at any given time.

Grieff Lacks "Concurrency":

Grieff's disclosure cannot support accepting commands concurrently because the commands, in Grieff appear to be stored in the Host FIS Buffer and FIS Command Decoder120, which is shown to receive only one input and that input is from the switch 110 coupling the command. Thus, there does not appear to be any way to achieve concurrent acceptance of commands, at any time, even at idle times by the disclosure of Grieff.

Furthermore, in Grieff, because only the Host FIS Buffer & FIS Command decoder 120 stores received commands and also apparently decodes received commands [See Grieff: Col. 5, lines 27-28 and Col. 7, lines 9-13], it is believed that Grieff can only receive and detect one command at any given time.

In Grieff, the state machines in Figs. 2-10 appear to offer further details of the Command Tracker SM 114 of Fig. 1. For example, in Grieff, there is stated "At step 1012, the link layer enters a loop that waits to receive an XRDY primitive. At step 1014, the link layer enters a loop that waits for FIS buffer to become available" [Grieff: Col. 16, lines 57-59]. Therefore, since the FIS buffer, in Grieff, stores the current command and the current command must be processed while in the FIS buffer before the FIS buffer becomes available, another command cannot possibly be received, at least not according the disclosure of Grieff. Completion of a command is detected by the SM 114. [Grieff: Col. 6, lines 16-26] Furthermore, in Grieff, only after a command has been completed, can a new arbitration cycle begin [See Grieff: Col. 7, lines 2-6].

Moreover, in Grieff, the host ports 130 and 132 are Link Layer (layer 2) state machines for relaying primitives with no storage capability. [Grieff: Col. 5, lines 50-56.]

2. Brief Introduction to *Utsunomiya*

Utsunomiya relates to a single host and single device system using the older ATA (retroactively renamed parallel ATA or "PATA") interface. Unlike the small computer system interface (SCSI), PATA does not support command queuing, which means that a CPU or host must issue commands one at a time. [See: Utsunomiya, ¶[0004]]. Utsunomiya addresses this limitation by using a task file queue, stored either in the main memory or a host bus adapter (HBA). [Utsunomiya ¶[0020]]. Utsunomiya deals solely with a PATA interface, therefore the task file queue described in Utsunomiya conforms to the PATA protocol not the SATA protocol.

3. Brief Introduction to "Serial ATA Spefification"

The Serial ATA Specification is document that sets forth the technical specifications of the industry adopted for SATA interface protocol.

4. Brief Introduction to *Shin*

Shin discloses a serial communications architecture using packet ordering based on certain information.

5. Brief Introduction to *Boucher*

Boucher relates to a network interface card (NIC) technology.

Boucher discloses an intelligent NIC (INIC) to offload from the CPU, certain network processing tasks that are CPU intensive. The offloaded tasks have a propensity to cause the CPU to remain idle while, for example, waiting for RAM access. Boucher teaches an INIC that handles, inter alia, header processing, data copying, and checksumming.

B. Factual and Legal Discussions

1. The Combination of Utsunomiya and Grieff Do Not Render the Claimed Invention Obvious and Therefore Unpatentable

The combination of Utsynomiya and Grieff does not disclose "an arbitration and control circuit, …, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state" because, among other reasons, Grieff's host ports are state machines and not storage devices and Utsunomiya's design does not have a switch. There is no disclosure regarding task files or any type of storage queuing device being placed prior to the switch in Grieff. Utsunomiya certainly does not suggest anything of the like. Additionally, the combination does not process commands, from the host, in layer (or level) 4 of the SATA protocol.

Therefore, the combination cannot perform the concurrent access to the device by the host of the claimed invention. Specifically, in the claimed invention, the first and second task files are each separately responsive to commands from the first and second host units, respectively. Thus, they concurrently accept commands, even when the device is non-idle. The claimed subject matter is capable of such concurrent acceptance of commands at least in part due to the task files and processing of the commands in other than layer 2 (the link layer) and arbitrating only after commands have been stored in the task files. As claimed,

"a first serial advanced technology attachment (SATA) port including a first host task file, coupled to a first host unit, the first host task file responsive to commands sent by the first host unit, to the device; a second serial ATA port, coupled to a second host unit including a second host task file, the second host task file responsive to commands sent by the second host unit, to the device; a third serial ATA port, coupled to a device, for causing access, by the first or second host units, to the device; and an arbitration and control circuit for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state." [Claim 1].

The foregoing is in sharp contrast with the combination of Grieff and Utsunomiya. The arbiter module 112 in Grieff appears to identify a host for exclusive access to the device. When one

host has won arbitration, it has exclusive access to send a command to the dual port adaptor. The other host must wait until the command is completed and the device is idle to send a command. [See Grieff: Col. 5, Lns. 56-62 and Col. 7, Lns. 2-6.] Utsunomiya lacks any type of arbitration as it only has one host. Thus, the combination does not work, nor allows for concurrent access by the two host units.

Additionally, the combination simply will not work in a manner consistent with "selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state". The host ports of Grieff 130 and 132 are Link Layer (layer 2) ports, the task file (which is at the application layer) queue of Utsunomiya cannot be placed in host ports 130 and 132 of Grieff. It is noted that SATA uses a multi-layer communication protocol with four layers, each with different functionality. SATA Specification ver. 2.6 (February 15, 2007) 42-43. To properly interact, components must operate on the same layer: a component operating on the Link Layer (layer 2) cannot operate on the Command Layer (layer 4). SATA Specification ver. 2.6 (February 15, 2007) 42-43. Even assuming *arguendo* that the arbiter module of Grieff can be redesigned to work in layer 4, redesigning the arbiter module 112 would in turn require re-engineering each subsequent component to interact with Command Layer (layer 4) at the host ports 130, 132. It is not clear whether any of the above reengineering will even work.

Thus, the host ports 130, 132 of Grieff cannot interface with the TFQs from Utsunomiya which function at the Parallel ATA (PATA) Application Layer. It is believed that the combination forming the basis of the foregoing rejections is not operational relative to the claimed invention and therefore do not render the claimed invention obvious.

2. The Claimed Invention is Not Obvious Because the Proposed Combination of References Simply Does Not Work

The Office Action of March 3, 2007 states that "it would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya's task file

queue (TFQ) into Grieff's ATA ports for the benefit of decreasing the work load of the host unit for issuing commands." Office Action of March 3, 2007, page 6.

In fact, the combination does not work. The host ports 130 and 132 in Grieff operate at the Link Layer (layer 2). In comparison, the TFQs from Utsunomiya function in PATA protocol, which is basically an Application Layer.

By way of brief background, SATA is generally a four-layer protocol, comprising a physical layer, a link layer (or layer 2), a transport layer, and an application layer (or layer 4). In SATA, the basic unit of communication or exchange is a frame. A frame comprises of a start of frame (SOF) primitive, a frame information structure (FIS), a Cyclic Redundancy Checksum (CRC) and an end of frame (EOF) primitive.

Thus, SATA uses a multi-layer communication protocol with four layers, each with different functionality. [See: SATA Specification ver. 2.6 (February 15, 2007) 42-43]. To properly interact, components must operate on the same layer: a component operating on the link layer (or layer 2) cannot operate on the command layer (layer 4). [See: SATA Specification ver. 2.6 (February 15, 2007) 42-43]. It is noted that command layer and application layer refer to the same layer.

Thus, the link layer host ports 130 and 132 of Grieff, lacking storage capability, can neither store nor interface with the application layer TFQs from Utsunomiya.

Furthermore, the arbiter module 112 of Grieff processes at the Link Layer (layer 2) rather than the command layer (layer 4). [See: Grieff, Col. 5, Lns. 50-56]. Redesigning the arbiter module 112 would in turn require re-engineering each subsequent component to interact with command layer (layer 4) at the host ports 130, 132. Without redesigning each subsequent component the system simply would not work.

In short, simply "including" Utsunomiya's TFQs into Grieff's ATA ports will not work because at least the following sub-systems will need to be re-engineered or eliminated:

- The ports 130, 132 in Grieff. As recited, these ports don't have storage capability to handle TFQs.

- Utusunomiya's TFQ 22. As recited, the TFQ 22 is "done in software" and resides in RAM 16. Furthermore, it functions in PATA, and is not compatible with SATA FIS.

- Grieff's OR Table 116. If routing of non-data FIS were transparent to the switch, much of the functionality of this sub-system would be rendered useless, but it's unclear that the OR Table could simply be removed.

- Grieff's decoder 120. Much of the functionality of this sub-system would be rendered useless by the TFQs, but it's unclear that the decoder could simply be removed.

- Grieff's decoder command tracker SM 114. This state machine accepts and generates control signals for numerous sub-systems that have to be re-engineered or eliminated. Therefore, Figs. 2 through 8 in Grieff, showing the various states in the command tracker state machine 114, would have to be substantially re-engineered.

3. The Claimed Invention is Not Obvious Because the Proposed Combination Teaches Away

In Grieff, the host ports 130 and 132 do not have storage capability. [Grieff: Col. 5, lines 50-56.] In fact, received commands are received and stored in the Host FIS Buffer & FIS Command decoder 120, which is situated after the arbiter module 112 and switch 110 thereof. [See Grieff: Col. 5, lines. 27-28 and Col. 7, lines 9-13 and Fig. 1]. Utsunomiya only has a single port. Accordingly, the combination teaches away from task files included in each host port allowing for concurrency, as in the claimed invention.

4. The Claimed Invention is Not Obvious Because the Advantages Offered by the Claimed Invention Are Not Realized By The Proposed Combination of References

The claimed invention offers the advantage of "concurrency" over the combination. The concurrent acceptance of commands by multiple hosts offers advantages over the combination for various reasons including system reliability. For example, when a host fails, due to acceptance of commands from any of the hosts, other hosts resume without any glitches or disruptions to the system. [See Specification: Page 42, line 25 to page 44, line 11.] Neither Grieff nor Utsunomiya offer this advantage. The combination of Grieff and Utsunomiya similarly does not offer this advantage.

Additionally, the delay through the switch of the claimed invention is reduced because "the second layer of the SATA link is employed as opposed to only the first layer. The switch is actually a layer 2 switch, thus, capable of communicating within the link layer as well as the physical layer" [See Specification: Page 44, line 7 – line 11]. Neither Grieff nor Utsunomiya offer this advantage. The combination of Grieff and Utsunomiya similarly does not offer this advantage.

Moreover, the switch of the claimed invention is capable of communicating within the link layer as well as the physical layer. [See Specification: Page 44, lines 10-11]. Neither Grieff nor Utsunomiya offer this advantage. The combination of Grieff and Utsunomiya similarly does not offer this advantage.

Due to the host ports 130 and 132 and the arbiter module 112 being exclusively Link Layer (layer 2) state machines with no storage capability and Utsunomiya operating in a single layer, as specified by the PATA standard, the combination cannot offer the foregoing advantages. [Grieff: Col. 5, lines 50-56].

5. The Combination of Utsunomiya and Grieff Fails to Specify Whether SATA or PATA Would be Used

As a separate basis of patentability, combining Utsunomiya and Grieff are believed to be wrong because the latter discloses a system using the serial ATA (SATA) standard and the former discloses a system using the ATA standard and there is no suggestion of one as to standard of the other. These two standards are very different. Among their differences are: SATA uses a serial link that uses Gigabit technology and 8b/10b encoding for connectivity whereas ATA uses a parallel bus; and The architecture of SATA is based on four layers of communication: Application, Transport, Link, and Physical whereas only one layer (Application) of communication is used in ATA. To combine the foregoing standards would be to re-design the systems. The claimed invention is directed to a system using the SATA standard, which is not disclosed by Utsunomiya.

6. The Standard for Obviousness Analysis

The standard for obviousness analysis is set forth in KSR International Co. v. Teleflex Inc., 127 S. Ct. 1727 (2007). In KSR, the Court held that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art…Inventions in most, if not all, instances rely upon building blocks long since uncovered and claimed discoveries almost of necessity will be combinations of what . . . is already known." [Id at 1741].

In analyzing obviousness the Court further held that an invention is obvious where "a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." (emphasis added) [Id. at 1742]. Here, the combination of elements from Grieff and Utsunomiya cannot simply be put together like a puzzle to yield the claimed invention.

That is, for the foregoing reasons, among others, the TFQs of Utsunomiya *cannot* simply be inserted into the host ports of Grieff.

Any combination of these elements would require, if can be done at all, re-engineering to such an extent as to render them practically unrecognizable.

Appellants thus submit that the cited combination lacks an element of the claimed invention, and that any combination will not work without re-engineering the art beyond recognition.

Obviousness Analysis and a Combination of References

In In re Keller, 642 F. 2d 413, 425 (CCPA 1981), the Court held that when combining reference teachings to support a rejection" it is not necessary that a device shown in one reference can be physically inserted into the device shown in the other." The Court further held that "the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." Id.

The Court in In re Merck & Co., 80 F. 2d 1091, 1097 (Fed. Cir. 1986) held that non-obviousness cannot be established by attacking references individually where the rejections are based upon combinations of references.

Applying this to the claimed invention, Utsunomiya certainly does not teach a switch, as there are none required for a single-host system, and Grieff does not teach multiple hosts accessing a device concurrently, as claimed. It is therefore submitted that under the In re Keller and/or Merck test, the combined teachings of the references would not have suggested to those of ordinary skill in the art the claimed subject matter.

Undue Burden Upon the Person Having the Ordinary Skill in the Art

The combination of Utsunomiya and Grieff cited by the examiner would place an undue burden on the hypothetical person having the ordinary skill in the art (PHOSITA). Significant re-design and substantial alteration of the combined references would be required to yield the claimed subject matter. Such an effort is well beyond what can reasonably be attributed to the PHOSITA, thereby creating an undue burden. The redesign required of the task file queues (TFQ) in the combined references illustrates this undue burden. The ports 130 and 132 in Grieff do not have storage capacity nor do they operate in other than the link layer . Therefore, the PHOSITA would need to redesigned them significantly, imposing undue burden, to allow for the acceptance of TFQs.

Utsunomiya's TFQ is executed in software, and resides in RAM. Additionally, Utsunomiya employs the PATA standard, and interfaces in the application layer (layer four), while the host ports of Grieff interface using the link layer (layer two). The above required changes go beyond simply "[pursuing] known options within his or her technical grasp." KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1724 (2007).

7. The Examiner Improperly Used Hindsight in His Finding of Obviousness

When the Board does not explain the motivation suggestion or teaching that would have led the skilled artisan at the time of the invention to the claimed combination as a whole, an

inference is created that hindsight was used to find obviousness. [In re Kahn, 441 F.3d 977, 986].

Here, the Examiner has failed to meet this requirement. Thus, an inference of hindsight is created. The use of hindsight to reject an application as obvious is impermissible. KSR, supra at 1742.

Appellants further submit that improper hindsight was used in the obviousness rejection, and that a *prima facie* case for obviousness has not been made.

8. The Claimed Invention and the Prior Art References Grieff and Utsunomiya Sought to Solve Different Problems

The subject invention sought to increase system stability. Because the first and second task files are each separately responsive to commands from the first and second host units, they are able to concurrently accept commands, even when the device is non-idle, which improves system performance by making command acceptance transparent to the hosts allowing the latter to send hosts at any time. In the event a host fails, due to acceptance of commands from any of the hosts, other hosts resume without any glitches or disruptions to the system. In this manner, the subject invention set out to improve system stability. [See Specification: Page 42, line 25 to page 44, line 11]

The problems sought to be addressed in both Grieff and Utsunomiya are not concerned with system stability. While Grieff sought to enable multiple hosts to access a single SATA device, it did not seek to do so concurrently while improving system performance because a pending host command needs to be completed prior to acceptance of another command from another host. Utsunomiya sought to decrease the work load of a single host by utilizing an interface apparatus to allow the CPU to issue a plurality of commands at the same time. Neither Grieff nor Utsunomiya sought to improve system stability and performance.

9. A Prima Facie Case of Obviousness Has Not Been Established Because the Examiner Has Not Considered the Level of Ordinary Skill in the Pertinent Art, or Stated a Motivation to Combine the Cited References

In re Kahn, 441 F.3d 977 (Fed. Cir. 2006) sets forth the requirement for a *prima facie* showing of obviousness. Under Kahn, a *prima facie* case is made where "both the scope and content of the prior art and [the] level of ordinary skill in the pertinent art" are considered. *Id.* at 986. Furthermore, in rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. [See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)]. In so doing, the examiner is expected to explain the reason(s) why one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious. This entails consideration of both the "scope and content of the prior art" and "level of ordinary skill in the pertinent art." In re Kahn, 441 F.3d 977, 986, cited by the Supreme Court in KSR International v. Teleflex 127 S. Ct. 1727, 1740.

The Examiner cannot simply reach conclusions based on the examiner's own understanding or experience – or on his or her assessment of what would be basic knowledge or common sense. Rather, the Examiner must point to some concrete evidence in the record in support of these findings. [In re Zurko, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 200 1)]. Thus the Examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the Examiner's conclusion. These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. [See: In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)].

We respectfully submit that the Examiner has clearly not met this burden.

In fact, nothing in Grieff teaches, suggests, or hints at including a task file queue in the host ports. To do so not only requires hindsight, but would also require at least re-designing practically all of Grieff, if it would work at all. It would also require re-designing the TFQ of Utsunomiya.

In particular, in rejecting Claim 1, the Examiner has failed to describe the level of ordinary skill in the pertinent art. Furthermore, the Examiner finds the mere awareness of a task file queue as sufficient motivation to extend the disclosures of Utsunomiya into Grieff to provide the features in the claimed invention.

Independent claims 18 and 31 each, at least substantially parallel, claim 1 and are thus believed to be necessarily allowable for, inter alia, the foregoing reasons with respect to claim 1.

Claims 4-17 are also allowable at least as depending from the allowable base claim 1.

Claims 19 and 22-30 are also allowable at least as depending from the allowable base claim 18.

Claims 32 and 35-43 are also allowable at least as depending from the allowable base claim 31.

C. Conclusion

Appellants thus submit that the combination art of record fails to establish proper rejections. Appellants therefore respectfully request the reversal of all the rejections under 35 U.S.C. § 103, at least for the reasons noted above.

Respectfully submitted,
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I hereby certify that this correspondence with all attachments is being electronically filed with the U.S. Postal Service and addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450 on March 14 , 2008 by Maryam Imam.

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IX. LISTING OF CLAIMS

Claim 1 (previously presented): A switch coupled between a plurality of host units and a device for communicating therebetween and comprising:

a) a first serial advanced technology attachment (ATA) port coupled to a first host unit and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;

b) a second serial ATA port coupled to a second host unit and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;

a third parallel ATA port, coupled to a device, for causing access to the device, by the first or second host units; and

an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Claim 2 (canceled).

Claim 3 (canceled).

Claim 4 (previously presented): A switch as recited in claim 1 wherein said third parallel ATA port includes a device task file.

Claim 5 (original): A switch as recited in claim 4 wherein said first, second and third ports are level 4 ports.

Claim 6 (original): A switch as recited in claim 1 wherein said device is a storage unit.

Claim 7 (original): A switch as recited in claim 1 wherein said switch is employed in an enterprise system.

Claim 8 (original): A switch as recited in claim 1 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 9 (original): A switch as recited in claim 1 wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units.

Claim 10 (original): A switch as recited in claim 9 wherein the information is referred to as 'identity drive response'.

Claim 11 (original): A switch as recited in claim 9 wherein the information is referred to as 'Tag.

Claim 12 (original): A switch as recited in claim 1 wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device.

Claim 13 (original): A switch as recited in claim 12 wherein the information is referred to as 'Tag'.

Claim 14 (original): A switch as recited in claim 13 wherein the arbitration and control circuit include a Tag/Sactive Mapping Circuit for mapping a host tag to a device tag and inverse mapping for identifying a host.

Claim 15 (original): A switch as recited in claim 1 wherein either the first or the second host sends a legacy queue command queued by the device.

Claim 16 (original): A switch as recited in claim 1 wherein either the first or the second host sends a native queue command for execution thereof by the device.

Claim 17 (original): A switch as recited in claim 1 wherein the first, second and third ports are level 3 ports and a Data frame information system (FIS) first-in-first-out (FIFO) and an associated FIFO Control are coupled to the first, second and third ports and located external thereto.

Claim 18 (previously presented): A switch comprising:

a first serial advanced technology attachment (ATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA port for connection to a device; and

an arbitration and control circuit, coupled to the first, second and third ports, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Claim 19 (original): A switch as recited in claim 18 wherein the switch is a serial ATA switch.

Claim 20 (cancel).

Claim 21 (cancel).

Claim 22 (currently amended): A switch as recited in claim [[21]] 18 wherein said third parallel ATA port includes a device task file.

Claim 23 (original): A switch as recited in claim 18 wherein said device is a storage unit.

Claim 24 (original): A switch as recited in claim 18 wherein said switch is employed in an enterprise system.

Claim 25 (original): A switch as recited in claim 18 wherein said arbitration circuit causes concurrent access of the device by the first and second host units.

Claim 26 (original): A switch as recited in claim 18 wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units.

Claim 27 (original): A switch as recited in claim 26 wherein the information is referred to as 'identity drive response'.

Claim 28 (original): A switch as recited in claim 26 wherein the information is referred to as 'Tag".

Claim 29 (original): A switch as recited in claim 18 wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device.

Claim 30 (original): A switch as recited in claim 28 wherein the information is referred to as 'Tag'.

Claim 31 (previously presented): A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, said switch comprising:

a first serial ATA port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host_unit;

a second serial ATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA port for connection to a device; and

d. an arbitration and control circuit, coupled to the first, second and third ports, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state.

Claim 32 (original): A switch as recited in claim 31 wherein the switch is a serial ATA switch.

Claim 33 (cancel).

Claim 34 (cancel).

Claim 35 (currently amended): A switch as recited in claim [[34]] 31 wherein said third parallel ATA port includes a device task file.

Claim 36 (original): A switch as recited in claim 31 wherein said device is a storage unit.

Claim 37 (original): A switch as recited in claim 31 wherein said switch is employed in an enterprise system.

Claim 38 (original): A switch as recited in claim 31 wherein said arbitration and control circuit causes concurrent access of the device by the first and second host units.

Claim 39 (original): A switch as recited in claim 31 wherein information, in the form of data, commands or setup, is transferred from the device to the first or second host units through the switch and the information is modified by the switch prior to being received by the first or second host units such that modified information rather than the information is received by the first or second host units.

Claim 40 (original): A switch as recited in claim 39 wherein the information is referred to as 'identity drive response'.

Claim 41 (original): A switch as recited in claim 39 wherein the information is referred to as 'Tag'.

Claim 42 (original): A switch as recited in claim 31 wherein information, in the form of data, commands or setup, is transferred from the first or second host units to the device through the switch and the information is modified by the switch prior to being received by the device such that modified information rather than the information is received by the device.

Claim 43 (original): A switch as recited in claim 42 wherein the information is referred to as 'Tag'.

X. APPENDIX

A. EVIDENCE APPENDIX: None
B. RELATED PROCEEDINGS APPENDIX: None